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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/055,499	01/22/2002	Jin-Yuan Lee	JCLA8534	7456

7590 05/03/2004

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EXAMINER	
THAI, LUAN C	
ART UNIT	**PAPER NUMBER**
2827	

DATE MAILED: 05/03/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/055,499	LEE ET AL.	
	Examiner	Art Unit	
	Luan Thai	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *61-63,70-81,83-93 and 95-100* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *61-63,70-81,83-93 and 95-100* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 January 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election of Embodiment I of Figs. 1-1i with claims 61-63, 70-81, 83-93, and 95-100 being read on the elected Embodiment, dated 3/5/04, is acknowledged. Claims 64-69, 82, 94, and 101-175 are canceled. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a).

Priority

2. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 61-62, 72-76, 78, 83-90, and 95, are rejected under 35 U.S.C. 102(b) as being anticipated by Saito et al (5,049,980).

The figures and reference numbers referred to in this office action are used merely to indicate an example of a specific teaching and are not to be taken as limiting.

Regarding claims 61-62, 72-76, 78, 83-90, and 95, Saito et al (see specifically figures 1-5) disclose a chip packaging method comprising: providing an organic substrate (1) with a surface; providing a plurality of dies (2), wherein each die has an active surface, a backside that is opposite to the active surface, and a plurality of metal pads (3) located on the active surface, whereas the backside of each die is adhered to the surface of the organic substrate; allocating a first dielectric layer (4) of polyimide on top of the surface of the substrate (1) and the active surface of the dies (2), and patterning the first dielectric layer (4) to form a plurality of first thru-holes (5) (see figure 2); filling the thru-holes (5) with a conductive material to form a plurality of first vias (6), puttering a first patterned wiring layer (7) on top of the first dielectric layer (4), wherein the first patterned wiring layer (7) is electrically connected to the metal pads (3) of the dies (2) through the first dielectric layer (4) by the vias (6) and extends to a region outside of an area above the active surfaces of the dies; allocating a second dielectric layer (9) on top the first dielectric layer and the first patterned wiring layer; allocating a second patterned wiring layer (11) on top the second dielectric layer (9), wherein the second patterned wiring layer is electrically connected to the first patterned wiring layer (7) via conductive vias (10) formed through the second dielectric layer (9), and the second patterned wiring layer extends to a region outside the active surface of the die and has a plurality of second bonding pads.

5. Claims 61-62, 70-73, 75-79, 83-85, 87-91, and 95-98, are rejected under 35 U.S.C. 102(e) as being anticipated by Wachtler et al (6,274,391).

The figures and reference numbers referred to in this office action are used merely to indicate an example of a specific teaching and are not to be taken as limiting.

Regarding claims 61-62, 70-73, 75-79, 83-85, 87-91, and 95-98, Wachtler et al (see specifically figures 8-22) disclose a chip packaging method comprising: providing an organic substrate (12) with a surface; providing a plurality of dies (16)/(52) (Col. 11, lines 41-67 and Col. 12, lines 1-9), wherein each die has an active surface, a backside that is opposite to the active surface, and a plurality of metal pads (Col. 8, lines 63-67) located on the active surface, whereas the backside of each die is adhered to the surface of the organic substrate by a adhesive (Col. 8, lines 53+); allocating a filling layer on top of the surface of the substrate and surrounding the peripheral of the dies (Col. 8, lines 59+) and a top surface of the filling layer being planar to the active surface of the dies (Col. 8, lines 64+); allocating a first dielectric layer (26/24) of polyimide on top of the surface of the substrate (12) and the active surface of the dies (16), and patterning the first dielectric layer to form a plurality of first thru-holes (28) (see figures 11-12); depositing a first patterned wiring layer (34) on top of the first dielectric layer (24/26), wherein the first patterned wiring layer fills the first thru-holes (28), is electrically connected to the metal pads of the dies (16), extends to a region outside of an area above the active surfaces of the dies, and has a plurality of first bonding pads (32). Wachtler et al further disclose allocating a

second dielectric layer (36/38) on top of the first dielectric layer (24/26) and the first patterned wiring layer (34); forming a plurality of second thru-holes (40) through the second dielectric layer (see figures 16-17); allocating a second patterned wiring layer (42) on top the second dielectric layer, wherein the second patterned wiring layer is electrically connected to the first patterned wiring layer through the second dielectric layer, and the second patterned wiring layer extends to a region outside the active surface of the die and has a plurality of second bonding pads (44); allocating a patterned passivation layer (46) on top of the second dielectric layer and the second patterned wiring layer and exposing the second bonding pads (44); attaching solder balls (22) to the binding pads (44).

6. Claims 61-62, 70-73, 75-81, 83-85, 87-93 and 95-100, are rejected under 35 U.S.C. 102(e) as being anticipated by Eichelberger et al (6,396,148).

The figures and reference numbers referred to in this office action are used merely to indicate an example of a specific teaching and are not to be taken as limiting.

Regarding claims 61-62, 70-73, and 75-79, Eichelberger et al (see specifically figures 1-7) disclose a chip packaging method comprising: providing an organic substrate (101) with a surface; providing a plurality of dies (102), wherein each die has an active surface, a backside that is opposite to the active surface, and a plurality of metal pads (107) located on the active surface, whereas the backside of each die is adhered to the surface of the organic substrate by a adhesive (103); allocating a filling layer (104) of polymer or epoxy

on top of the surface of the substrate (101) and surrounding the peripheral of the dies (102) and a top surface of the filling layer (104) being planar to the active surface of the dies (104) (see figures 3A and 4A); allocating a first dielectric layer (106) of polyimide on top of the surface of the substrate (101) and the active surface of the dies (102), and patterning the first dielectric layer (106) to form a plurality of first thru-holes (122) (see figures 3D and 4B); electro-less plating a first patterned wiring layer (109) on top of the first dielectric layer (106), wherein the first patterned wiring layer (109) is electrically connected to the metal pads (107) of the dies (102) through the first dielectric layer (106), extends to a region outside of an area above the active surfaces of the dies, and has a plurality of first bonding pads. Eichelberger et al further disclose: the first patterned wiring layer (109) extending into the first thru-holes (122) to electrically connect the first patterned wiring layer (109) and the metal pads (107) of the dies (102); allocating a patterned passivation layer (109) (or 232) on top of the first dielectric patterned wiring layer (108) (or 206) and exposing the first bonding pads on the first patterned wiring layer (108) for solder balls (110) electrically connected to, as disclosed in figure 1. (Noted that figures 6C-7C also disclose passivation layer "232" is formed on top of the first dielectric patterned wiring layer "206" and exposing the first bonding pads on the first patterned wiring layer "209" for solder balls "234" electrically connected to.

Regarding claims 80-81, Eichelberger et al also disclose a step of singularizing the chip package structure to form a single chip package (Col. 8, lines 46+).

Regarding claims 83-85, 87-93 and 95-100, Eichelberger et al further disclose that the steps of: a) allocating a second dielectric layer on top of the first dielectric layer and the first patterned wiring layer; b) allocating a second patterned wiring layer on top the second dielectric layer, wherein the second patterned wiring layer is electrically connected to the first patterned wiring layer through the second dielectric layer, and the second patterned wiring layer extends to a region outside the active surface of the die and has a plurality of second bonding pads; and c) other steps as described above can be repeated until all required metal layers have been completed (Col. 8, lines 53+).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 74 and 86 are rejected under 35 U.S.C. 103(a) as being unpatentable over Eichelberger et al (6,396,148) in view of Saito et al (5,049,980).

The figures and reference numbers referred to in this office action are used merely to indicate an example of a specific teaching and are not to be taken as limiting.

Regarding claims 74 and 86, Gottschall et al disclose all the limitations of the claimed invention, including the step of allocating the first (and second) patterned wiring layer (109) extending into the first (and second) thru-holes (122) to electrically connect the first (and second) patterned wiring layer (109) and the metal pads (107) of the dies (102), as detailed above. Gottschall et al, however, do not explicitly teach the step of filling the first and second thru-holes with a conductive material to form a plurality of first and second vias, by which the first and second wiring layers and the metal pads are electrically connected, as recited in claims 74 and 86, respectively.

Saito et al while related to a similar chip packaging method teach, among others, the steps of: filling the first and second thru-holes with a conductive material to form first conductive vias (6) and second conductive vias (10), which electrically connect the first and second wiring layers (7) and (11) to the metal pads (3) formed on the active surface of chips (2). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the method steps of Eichelberger et al in constructing the electrical connections between the multi-wiring layers on the semiconductor chips by using the step of filling the first and second thru-holes with a conductive material to form a plurality of first and second vias, by which the first and second wiring layers and the metal pads of the chip are electrically connected, since such method step is commonly applied in the semiconductor art for forming electrical connections among the

conductive wiring layers, as taught by Saito et al, and such modification is held to be within the ordinary designing ability expected of a person skilled in the art.

9. Claim 63 is rejected under 35 U.S.C. 103(a) as being unpatentable over Eichelberger et al (6,396,148, called "Eic-148") in view of Eichelberger et al (5,841,193, called "Eic-193").

The figures and reference numbers referred to in this office action are used merely to indicate an example of a specific teaching and are not to be taken as limiting.

Regarding claim 63, Eic-148 discloses all the limitations of the claimed invention including plurality of dies (102) provided and adhered to the surface of the substrate, as detailed above. Eic-148, however, does not explicitly teach the dies performing different functions.

Eic-193 while related to a similar chip packaging method teaches that the product formed by such method can comprise different dies (Col. 8, lines 55+). It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply Eic-148's method with the dies to perform different functions, since such application is commonly used in the art, as taught by Eic-193, and it is held to be within the ordinary designing ability expected of a person skilled in the art.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Luan Thai whose telephone number is 571-272-1935. The examiner can normally be reached on 6:45 AM - 4:15 PM, Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on 571-272-1957. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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